EXHIBIT A

Terms to Be Jointly Construed with Netlist, Inc. v. Micron Technology, Inc., et al., No. 1:22-cv-00134-LY

A. U.S. Patent No. 8,301,833 ("'833 Patent")

Claim Term	Plaintiff's Proposed	Plaintiff's Supporting Evidence	Defendants' Proposed	Defendants' Supporting Evidence
1. "volatile memory	Plain and ordinary	'833 Patent	"volatile memory	'833 Patent
subsystem" / "non-	meaning, as would be	• 7:8-11	subsystem" means "one	• 4:57-61
volatile memory	understood by one of	• 18:14-29	or more volatile memory	• 5:48-6:36
subsystem"	ordinary skill in the art in	• 18:33-44	devices."	• 7:66-8:56
('833 Pat., Cl. 15)	the context of the entire	• Fig. 1		• 10:43-58
	disclosure.	 Fig. 4A 	"non-volatile memory	• 12:53-55
			subsystem" means "one	• 13:57-14:47
		Declaration of Steven	or more non-volatile	• 15:59-16:37
		Przybylski, Ph. D.	memory devices.	• 17:18-21
				• 18:22-50
				• 19:20-26
				• 20:14-61
				• Fig. 1
				• Fig. 2
				• Fig. 3
				• Fig. 8
				SanDist Com v. Notlist
				Inc., IPR2014-00994,
				Paper 7 (Patent Owner
				Preliminary Response)
				(Opening Br., Ex. 14) at
				p. 12.

Claim Term	Plaintiff's Proposed Construction	Plaintiff's Supporting Evidence	Defendants' Proposed Construction	Defendants' Supporting Evidence
				SanDisk Corp. v. Netlist, Inc., IPR2014-00994,
				Paper 8 (Trial Institution Decision) (Opening Br.,
				Ex. 15) at p. 12.
				SMART Modular Tech.,
				Inc. v. Netlist, Inc., IPR2014-01370, Paper
				11 (Patent Owner
				Preliminary Response) (Onening Br. Fx. 16) at
				pp. 11-12.
				SMART Modular Tech.,
				Inc. v. Netlist, Inc.,
				IPR2014-01370, Paper 13 (Trial Institution
				Decision) (Opening Br., Ex. 17) at p. 16.
				SK hynix Inc. et al. v.
				Netust, Inc., IPR201/- 00649, Paper 6 (Patent
				Owner Preliminary
				Response) (Opening Br., Ev. 18) at n. 4
				LA: 10) at p. 1.

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Claim Term	Plaintiff's Proposed	Plaintiff's Supporting	Defendants' Proposed	Defendants'
2. "controller configured	Plain and ordinary	'833 Patent	This is a means-plus-	'833 Patent
to decouple the non-	meaning, as would be	• 2:46-49	function limitation.	Abstract
volatile memory	understood by one of	• 2:51-59		• 3:62-64
subsystem from the	ordinary skill in the art in	• 4:58-61	Function: entire	• 4:57-61
volatile memory	the context of the entire	• 4:63-64	limitation after	• 6:54-7:40
subsystem in the first	disclosure.	• 6:54-59	"configured to."	• 7:66-8:56
mode of operation and to		• 6:63-7:40	:	• 10:19-22
couple the non-volatile	Not subject to § 112, ¶ 6.	• 8:22-36	Corresponding Structure:	• 13:57-14:47
memory subsystem to		• 10:8-22	"controller that is	• 15:59-16:37
the volatile memory		• 10:55-58	separate from the volume	• 18:29-20:61
subsystem in the second		• 15:46-16:3	and non-volatile memory	• Fig. 1
mode of operation		• 22:12-17	subsystems, as	• Fig. 2
(633 Fat., Cl. 10)			Detent 6:63 7:40	• Fig. 3
		Declaration of Steven	ratent, 0.03-7.40.	• × × × × × × × × × × × × × × × × × × ×
		Przybylski, Ph. D.		
				SanDisk Corp. v. Netlist,
				Inc., IPR2014-00994,
				Paper 8 (Trial Institution
				Decision) (Opening Br.,
				Ex. 15) at p. 12.
				Declaration of Harold S
				Stone, Ph. D.

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A. U.S. Patent Nos. 9,824,035 and 10,268,608 ("Lee Patents")

Claim Term	Plaintiff's Proposed Construction	Plaintiff's Supporting Evidence	Defendants' Proposed Construction	Defendants' Supporting Evidence
1. "module control device"	Plain and ordinary meaning, as would be	<u>'035 Patent</u> • 1:40-2:35	This is a means-plus- function limitation.	Declaration of Alan Jay Smith, Ph. D. (No
('035 & '605 Pats., Cl. 1)	understood by one of	• 4:18-43		intrinsic evidence
	ordinary skill in the art in	• 4:63-5:8	Function: entire	because no
	the context of the entire	• 5:55-67	imitation after	corresponding structure)
	disclosure.	• 8:6-30	comignica to.	
	Neither indefinite nor	• 9:49-54 • Figs. 1, 2A, 2B,	Corresponding Structure:	
	subject to 8 112, 0.	2C, 2D, 7, 12A, 12B	corresponding structure	
		'608 Patent		
		• 1:43-2:36		
		• 4:20-35		
		• 4:65-5:10		
		• 5:58-6:3		
		• 8:9-34		
		• 9:52-57		
		• Figs. 1, 2A, 2B,		
		2C, 2D, 7, 12A,		
		12B		
		Declaration of Steven Przybylski, Ph. D.		

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Claim Term	Plaintiff's Proposed	Plaintiff's Supporting	Defendants' Proposed	Defendants'
	Construction	Evidence	Construction	Supporting Evidence
2. "logic"	Plain and ordinary	'035 Patent	This is a means-plus-	Declaration of Alan Jay
('035 Pat., Cl. 1)	meaning, as would be	• 4:18-33	function limitation.	Smith, Ph. D. (No
	understood by one of	• 5:40-54		intrinsic evidence
	ordinary skill in the art in	• 8:1-5	Function: entire	because no
	the context of the entire	• 8:18-30	limitation after	corresponding structure)
	disclosure.	• 9:27-29	"configured to." In	
		• 9:33-35	addition, the entire	'035 Patent
	Neither indefinite nor	• 9:42-48	limitation after "the logic	• 13:44-48
	subject to § 112, ¶ 6.	• 10:8-18	is further configured to."	• 14:60-65
		• 10:47-66	Corresponding Structure.	
		• 11:5-15	Indefinite – no	
		• 11:66-17:49	corresponding structure	
		• 18:9-15		
		• 18:63-19:7		
		• Figs. 3, 6, 8-19		
		Declaration of Steven		
		Przybylski, Ph. D.		
		Wilev Electrical and		
		Electronics Engineering		
		Dictionary (2004) (Ex. E		
		to Przybylski Decl.).		
3. "command processing	Plain and ordinary	'608 Patent	This is a means-plus-	Declaration of Alan Jay
circuit"	meaning, as would be	• 4:65-5:4	function limitation.	Smith, Ph. D. (No
('608 Pat., Cl. 1)	understood by one of	• 5:43-57		intrinsic evidence
	ordinary skill in the art in	• 10:50-11:7	Function: entire	because no
	the context of the entire	• 12:11-26	limitation after	corresponding structure)

Claim Term	Plaintiff's Proposed	Plaintiff's Supporting Defendants' Proposed Defendants'	Defendants' Proposed	Defendants'
	Construction	Evidence	Construction	Supporting Evidence
	disclosure.	• 14:57-17:54	"configured to" and	
		• 18:14-20	before "and a delay	
	Neither indefinite nor	• 19:1-12	circuit."	
	subject to § 112, ¶ 6.	• Figs. 3, 6, 7, 11A,		
		11B, 12A, 12B,	Corresponding Structure:	
		14-16, 19	Indefinite – no	
			corresponding structure	
		Declaration of Steven		
		Przybylski, Ph. D.		

B. U.S. Patent No. 10,489,314 ("'314 Patent")

Claim Term	Plaintiff's Proposed	Plaintiff's Supporting	Defendants' Proposed	Defendants'
	Construction	Evidence	Construction	Supporting Evidence
1. "burst of data strobes"	Plain and ordinary	'314 Patent	Indefinite.	'314 Patent
('314 Pat., Cls. 1, 15, 25,	meaning, as would be	• 3:17-4:30		• 13:18-23
28)	understood by one of	• 5:36		• Fig. 1
	ordinary skill in the art in	• 6:39-43		• Fig. 6A
	the context of the entire	• 7:28-48		• Fig. 6B
	disclosure. Not	• 13:18-51		• Fig. 7
	indefinite.	• 13:60-14:22		• Fig. 18
	,	• 14:41-56		• Fig. 19
	In the alternative	22.59		ò
	"strobe signals with	73:27		Declaration of Harold S.
	successive rising and	73:57		Stone Ph. D.
	falling edges, each edge	23.0/		
		6:97		
		• 31:35		

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Claim Term	Plaintiff's Proposed Construction	Plaintiff's Supporting Evidence	Defendants' Proposed Construction	Defendants' Supporting Evidence
	being associated with one or more data bits."	• 35:20-23 • Figs. 2, 6A, 6B, 7		
		Declaration of Steven Przybylski, Ph. D.		
		JESD79-2A (Ex. B to Przybylski Decl.) • pp. 26, 29, 30		
		JESD79-2B (Ex. C to Przybylski Decl.) • pp. 26, 29, 92- 103		
2. "logic" terms	Plain and ordinary	'314 Patent	This is a means-plus-	Declaration of Harold S.
(314 Fal., CIS. 1, 13, 23)	understood by one of	• Claims 1, 3, 13, 28	Tunction militation.	intrinsic evidence
	ordinary skill in the art in the context of the entire	• 5:64-67	Function Function For claim 1	because no corresponding structure)
	disclosure.	• 9:25-51	"respond[ing] to	0
	Neither indefinite nor	• 10:47-52	the first/second	
	subject to § 112, ¶ 6.	• 11:9-25 • 11:55-13:14	command by	
		• 15:19-24	providing	
		• 16:36-39	control signals to	
		• 10:00-03 • 17:20-28	the circuitry"	
		• 17:50-55		

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Claim Term	Plaintiff's Proposed Construction	Plaintiff's Supporting Evidence	Defendants' Proposed Construction	Defendants' Supporting Evidence
		 22:51-53 23:19-23 25:4-6 25:15-31:30 34:42-67 Verilog examples 1-3 Figs. 5A-5D, 9A-9B 	• For claims 15/25, "output[ting] first/second control signals to the circuitry in response to the first/second read or write memory command"	
		Declaration of Steven Przybylski, Ph. D.	Corresponding Structure: Indefinite – no corresponding structure.	
		Wiley Electrical and Electronics Engineering Dictionary (2004) (Ex. E to Przybylski Decl.).		
3. "overall CAS latency" / "actual operational CAS latency"	Plain and ordinary meaning, as would be understood by one of	**************************************	"overall CAS latency of the memory module" means "the delay	**************************************
('314 Pat., Cls. 1, 15, 25, 28)	ordinary skill in the art in the context of the entire disclosure.	7:20-269:34-4210:47-52	between: (1) the time when a read command is executed by the memory	Double Data Rate (DDR) SDRAM Specification, Standard
	In the alternative	15:26-3322:28-63	module, and (2) the time when the first piece of	No. 79, JEDEC Solid State Tech. Corp. (June
	"overall CAS latency of the memory module"	25:2525:44-27:829:16-20	data is made available at an output of the memory module"	2000) (Opening Br., Ex. 11) at pp. 10-11.

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Claim Term	Plaintiff's Proposed	Plaintiff's Supporting	Defendants' Proposed	Defendants'
	Construction	Evidence	Construction	Supporting Evidence
	means "the delay	• 31:34-40		DDR SDRAM Registered
	between: (1) the time	• 36:36-38	"actual operational CAS	DIMM Design
	when a command is	• 44:49-50	latency of each of the	Specification, Standard
	sampled on the memory	• 45:14	memory devices[/of each	No. 21-C, JEDEC Solid
	module, and (2) a time	• 45:19-20	of the plurality of	State Tech. Corp. (Rev.
	when the first piece of	 Verilog examples 	memory integrated	1.3, Jan. 2002) (Opening
	data is available at the	1-3	circuits]" means "the	Br., Ex. 12) at p. 68.
	data pins of the memory	 Figs. 3A-5D 	delay between: (1) the	Declaration of Harold S
	A Composition	Decloration of Ctorion	command is executed by	Stone. Ph. D.
	"actual operational CAS	Przyhylski Ph D	each of the memory	
	latency of each of the	1123 03 15111, 111 15.	devices[/each of the	
	memory devices[/of each	JESD79-2A (Ex. B to	plurality of memory	
	of the plurality of	Przybylski Decl.)	integrated circuits], and	
	memory integrated	• pp. 12, 24, 26	(2) the time when the	
	circuits]" means "the	•	first piece of data is	
	delay between: (1) the	Synchronous DRAM	made available at an	
	time when a command is	Architectures,	output of each of the	
	executed by each of the	Organizations, and	memory devices[/of each	
	memory devices[/each of	Alternative	of the plurality of	
	the plurality of memory	Technologies, by Prof.	memory integrated	
	integrated circuits], and	Bruce L. Jacob, dated	circuits]"	
	(2) a time when the first	December 10, 2002		
	piece of data is available	("Jacob Article") (Ex. D		
	at the data pins of each	to Przybylski Decl.)		
	of the memory	• p. 16		
	devices[/of each of the			
	plurality of memory	JESD79-2B (Ex. C to		
	integrated circuits]"	Przybylski Decl.)		
		• pp. 11-12, 24		

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Claim Term	Plaintiff's Proposed Construction	Plaintiff's Supporting Evidence	Defendants' Proposed Construction	Defendants' Supporting Evidence
4. "circuitry" terms	Plain and ordinary	'314 Patent	This is a means-plus-	Declaration of Harold S.
('314 Pat., Cls. 1, 15, 25,	meaning, as would be	• 5:53-67	function limitation.	Stone, Ph. D. (No
28)	understood by one of	• 7:20-27		intrinsic evidence
	ordinary skill in the art in	• 9:31-51	The identified "circuitry"	because no
	the context of the entire	• 19:36-50	teatures in claims 1, 15,	corresponding structure)
	disclosure.	• 22:38-63	25, and 28 are indefinite.	
		• 32:33-38	For claim 1 the	
		• Figs. 5A, 9A-9B,	"circuitry" feature is	
	subject to § 112, ¶ o.	10A-10B, 11A-	subject to § 112, ¶ 6, but	
		11B	there is no disclosure of	
		 Verilog examples 	adequate structure or	
		1-3	algorithm for the	
			functions of:	
			(i) enabl[ing] data	
			transfers through the	
			circuitry in response to	
			the first control signals;	
			(ii) enabl[ing] data	
			transfers through the	
			circuitry	
			subsequently in response	
			to the second control	
			signals; and	
			(iii) add[ing] a	
			predetermined amount of	
			time delay for each	
			registered data transfer	
			through the circuitry so	
			that the overall CAS	

Claim Term	Plaintiff's Proposed	Plaintiff's Supporting	Defendants' Proposed	Defendants'
	Construction	Evidence	Construction	Supporting Evidence
			latency of the memory	
			module is greater than an	
			actual operational CAS	
			latency of each of the	
			plurality of memory	
			integrated circuits.	
			The "circuitry" feature in	
			claim 15 is subject to §	
			112, ¶ 6, but there is no	
			disclosure of adequate	
			structure or algorithm for	
			the functions of:	
			(i) enabl[ing] data	
			transfers between the	
			first rank and the	
			memory bus through the	
			circuitry in response to	
			the first control signals;	
			and	
			(ii) add[ing] a	
			predetermined amount of	
			time delay for each	
			registered data transfer	
			through the circuitry	
			such that the overall	
			CAS latency of the	
			memory module is	
			greater than an actual	
			operational CAS latency	

Claim Term	Plaintiff's Proposed	Plaintiff's Supporting	Defendants' Proposed	Defendants'
	Construction	Evidence	Construction	Supporting Evidence
			of each of the memory	
			devices.	
			The additional	
			"circuitry" feature in	
			claim 25 is subject to §	
			112, \P 6, but there is no	
			disclosure of adequate	
			structure or algorithm for	
			the function of:	
			enabl[ing] registered	
			data transfers between	
			the second rank and the	
			memory bus through the	
			circuitry in response to	
			the second control	
			signals.	
			The "circuitry" feature in	
			claim 28 is subject to §	
			112, ¶ 6, but there is no	
			disclosure of adequate	
			structure or algorithm for	
			the functions of:	
			(i) add[ing] a	
			predetermined amount of	
			time delay for each data	
			transfer between the	
			memory controller and	
			the memory devices such	

Claim Term	Plaintiff's Proposed	Plaintiff's Supporting	Defendants' Proposed	Defendants'
	Construction	Evidence	Construction	Supporting Evidence
			that the overall CAS	
			latency of the memory	
			module is greater than an	
			actual operational CAS	
			latency of each of the	
			memory devices; and	
			(ii) the circuitry [of	
			claim 28] includ[ing]	
			logic pipelines	
			configured to enable data	
			transfers between the	
			first rank and the	
			memory bus in response	
			to the first read or write	
			memory command.	